

Z80™-PIO Z80A™-PIO



Product Specification

The Zilog Z-80 product line is a complete set of micro-computer components, development systems and support software. The Z-80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The Z-80 Parallel I/O (PIO) Interface Controller is a programmable, two port device which provides TTL-compatible interfacing between peripheral devices and the Z80-CPU. The Z80-CPU configures the Z80-PIO to interface with standard peripheral devices such as tape punches, printers, keyboards, etc.

Byte bidirectional bus (available on Port A only)
Bit Mode

- Programmable interrupts on peripheral status conditions.
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic.
- Eight outputs are capable of driving Darlington transistors.
- All inputs and outputs fully TTL compatible.

PIO Architecture

Structure

- N-Channel Silicon Gate Depletion Load technology
- 40 Pin DIP
- Single 5 volt supply
- Single phase 5 volt clock
- Two independent 8-bit bidirectional peripheral ports with "handshake" data transfer control

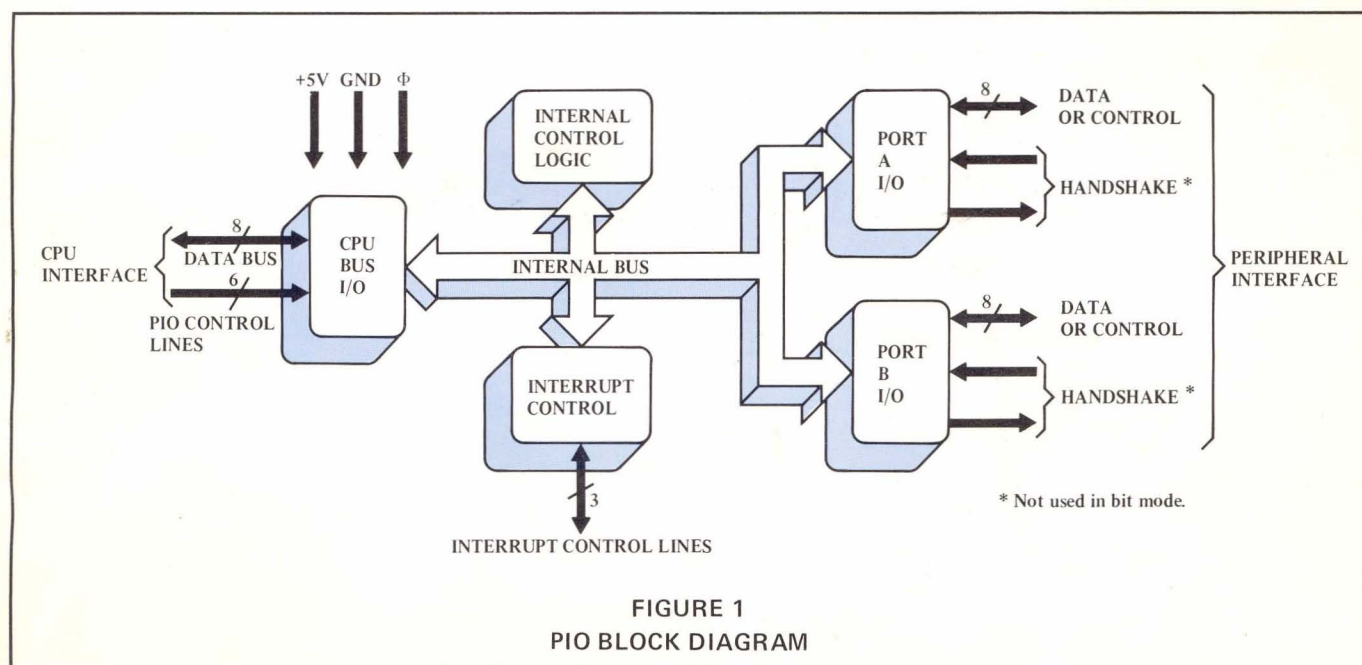
Features

- Interrupt driven "handshake" for fast response
- Any one of the following modes of operation may be selected for either port:
Byte output
Byte input

1977 Zilog Z80
PIO Product
Specby Marcus
1977 Zilog Z80
PIO Product
SpecBennett

Block diagram of the Z80-PIO is shown in figure 1. Internal structure of the Z80-PIO consists of a CPU bus interface, internal control logic, Port A I/O logic, Port B I/O logic, and interrupt control logic. An application might use Port A as the data transfer and Port B for the status and control monitoring.

Port I/O logic is composed of 6 registers with "handshake" control logic as shown in figure 2. The registers include: an 8-bit input register, an 8-bit output register, a 2-bit mode control register, an 8-bit mask register, an 8-bit input/output select register, and a 2-bit mask control register. The last three registers are used only when the port has been programmed to operate in the bit mode.



Register Description

Mode Control Register—2 bits, loaded by CPU to select the operating mode: byte output, byte input, byte bidirectional bus or bit mode.

Data Output Register—8 bits, permits data to be transferred from the CPU to the peripheral.

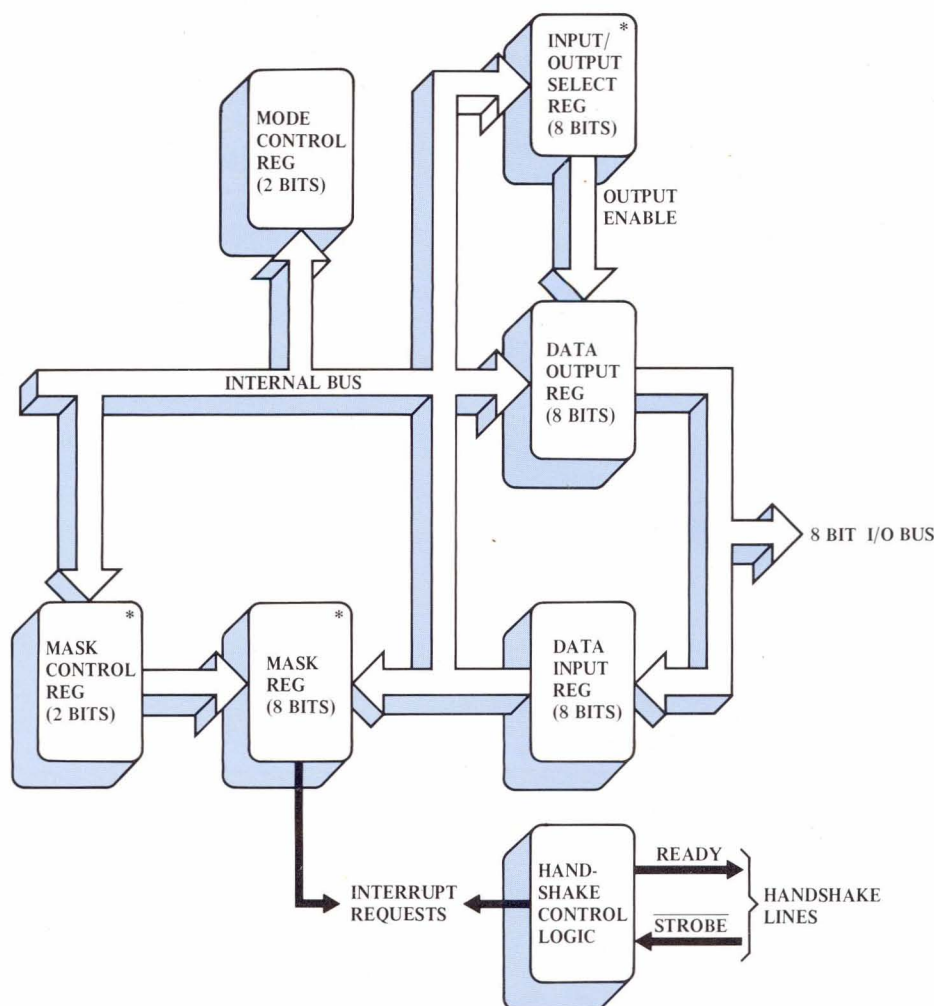
Data Input Register—8 bits, accepts data from the peripheral for transfer to the CPU.

Mask Control Register—2 bits, loaded by the CPU to specify the active state (high or low) of any peripheral device

interface pins that are to be monitored and, if an interrupt should be generated when all unmasked pins are active (AND condition) or, when any unmasked pin is active (OR condition).

Mask Register—8 bits, loaded by the CPU to determine which peripheral device interface pins are to be monitored for the specified status condition.

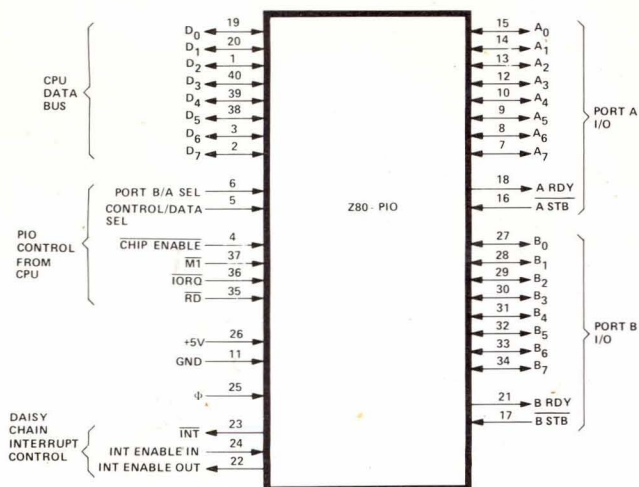
Input/Output Select Register—8 bits, loaded by the CPU to allow any pin to be an output or an input during bit mode operation.



* Used in the bit mode only to allow generation of an interrupt if the peripheral I/O pins go to the specified state.

FIGURE 2
A TYPICAL PORT I/O BLOCK DIAGRAM

Z80-PIO Pin Description



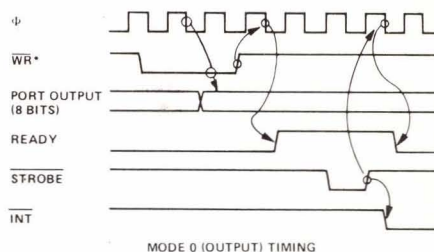
D ₇ -D ₀	Z80-CPU Data Bus (bidirectional, tristate)
B/A Sel	Port B or A Select (input, active high)
C/D Sel	Control or Data Select (input, active high)
CE	Chip Enable (input, active low)
Φ	System Clock (input)

$\overline{M1}$	Machine Cycle One Signal from CPU (input, active low)
\overline{IORQ}	Input/Output Request from Z80-CPU (input, active low)
\overline{RD}	Read Cycle Status from the Z80-CPU (input, active low)
IEI	Interrupt Enable In (input, active high)
IEO	Interrupt Enable Out (output, active high). IEI and IEO form a daisy chain connection for priority interrupt control.
\overline{INT}	Interrupt Request (output, open drain, active low)
A ₀ -A ₇	Port A Bus (bidirectional, tristate)
A STB	Port A Strobe Pulse from Peripheral Device (input, active low)
A RDY	Register A Ready (output, active high)
B ₀ -B ₇	Port B Bus (bidirectional, tristate)
B STB	Port B Strobe Pulse from Peripheral Device (input, active low)
B RDY	Register B Ready (output, active high)

Timing Waveforms

OUTPUT MODE

An output cycle is always started by the execution of an output instruction by the CPU. The \overline{WR} pulse from the CPU latches the data from the CPU data bus into the selected port's output register. The write pulse sets the ready flag after a low going edge of Φ , indicating data is available. Ready stays active until the positive edge of the strobe line is received indicating that data was taken by the peripheral. The positive edge of the strobe pulse generates an \overline{INT} if the interrupt enable flip flop has been set and if this device has the highest priority.

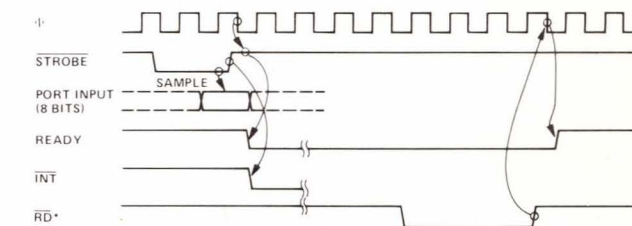


MODE 0 (OUTPUT) TIMING

$$\overline{WR}^* = \overline{RD} \cdot CE \cdot \overline{C/D} \cdot \overline{IORQ}$$

INPUT MODE

When STROBE goes low data is loaded into the selected port input register. The next rising edge of strobe activates \overline{INT} if interrupt enable is set and this is the highest priority requesting device. The following falling edge of Φ resets Ready to an inactive state, indicating that the input register is full and cannot accept any more data until the CPU completes a read. When a read is complete the positive edge of \overline{RD} will set Ready at the next low going transition of Φ . At this time new data can be loaded into the PIO.

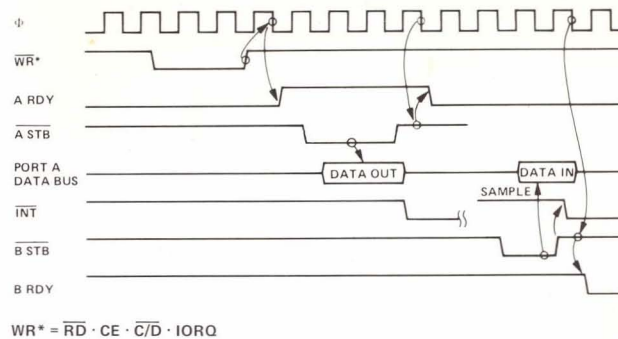


MODE 1 (INPUT) TIMING

$$\overline{RD}^* = \overline{RD} \cdot CE \cdot \overline{C/D} \cdot \overline{IORQ}$$

BIDIRECTIONAL MODE

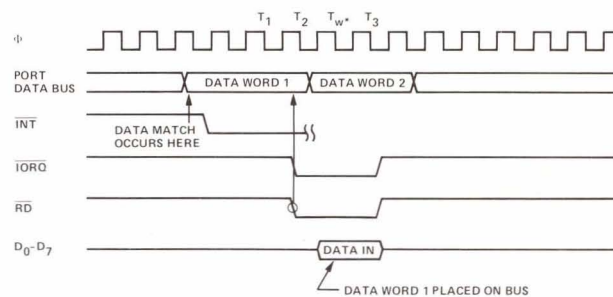
This is a combination of modes 0 and 1 using all four handshake lines and the 8 Port A I/O lines. Port B must be set to the Bit Mode. The Port A handshake lines are used for output control and the Port B lines are used for input control. Data is allowed out onto the Port A bus only when A STB is low. The rising edge of this strobe can be used to latch the data into the peripheral.



BIT MODE

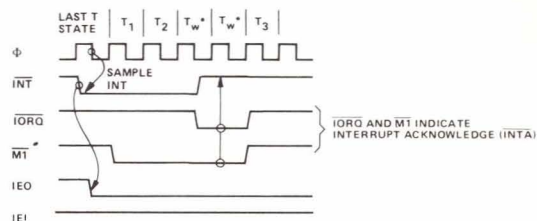
The bit mode does not utilize the handshake signals and a normal port write or port read can be executed at any time. When writing, the data will be latched into the output registers with the same timing as the output mode.

When reading the PIO, the data returned to the CPU will be composed of output register data from those port data lines assigned as outputs and input register data from those port data lines assigned as inputs. The input register will contain data which was present immediately prior to the falling edge of RD. An interrupt will be generated if interrupts from the port are enabled and the data on the port data lines satisfy the logical equation defined by the 8-bit mask and 2-bit mask control registers.



INTERRUPT ACKNOWLEDGE

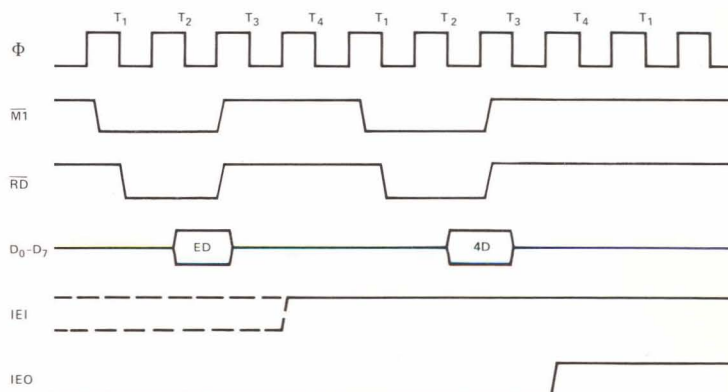
During MI time, peripheral controllers are inhibited from changing their interrupt enable status, permitting the INT Enable signal to ripple through the daisy chain. The peripheral with IEI high and IEO low during INTA will place a preprogrammed 8-bit interrupt vector on the data bus at this time. IEO is held low until a return from interrupt (RETI) instruction is executed by the CPU while IEI is high. The 2-byte RETI instruction is decoded internally by the PIO for this purpose.



RETURN FROM INTERRUPT CYCLE

If a Z80 peripheral device has no interrupt pending and is not under service, then its IEO=IEI. If it has an interrupt under service (i.e., it has already interrupted and received an interrupt acknowledge) then its IEO is always low, inhibiting lower priority chips from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO will be low unless an "ED" is decoded as the first byte of a two byte opcode. In this case, IEO will go high until the next opcode byte is decoded, whereupon it will again go low. If the second byte of the opcode was a "4D" then the opcode was an RETI instruction.

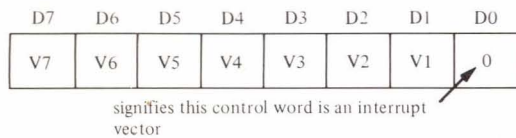
After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service will have its IEI high and its IEO low. This device is the highest priority device in the daisy chain which has received an interrupt acknowledge. All other peripherals have IEI=IEO. If the next opcode byte decoded is "4D", this peripheral device will reset its "interrupt under service" condition.



PIO Programming

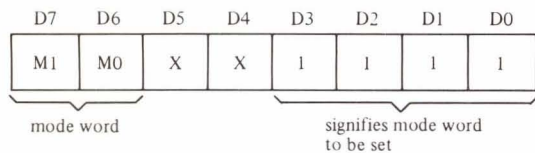
LOAD INTERRUPT VECTOR

The Z80-CPU requires an 8-bit interrupt vector be supplied by the interrupting device. The CPU forms the address for the interrupt service routine of the port using this vector. During an interrupt acknowledge cycle the vector is placed on the Z-80 data bus by the highest priority device requesting service at that time. The desired interrupt vector is loaded into the PIO by writing a control word to the desired port of the PIO with the following format.



SELECTING AN OPERATING MODE

When selecting an operating mode, the 2-bit mode control register is set to one of four values. These two bits are the most significant bits of the register, bits 7 and 6; bits 5 and 4 are not used while bits 3 through 0 are all set to 1111 to indicate "set mode."



X=unused bit

Mode	M ₁	M ₀
Output	0	0
Input	0	1
Bidirectional	1	0
Bit	1	1

MODE 0 active indicates that data is to be written from the CPU to the peripheral.

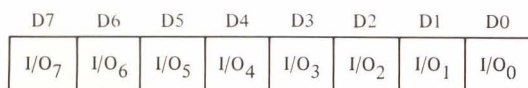
MODE 1 active indicates that data is to be read from the peripheral to the CPU.

MODE 2 allows data to be written to or read from the peripheral device.

MODE 3 is intended for status and control applications. When selected, the next control word must set the I/O Register to indicate which lines are to be input and which lines are to be output.

I/O = 1 sets bit to input.

I/O = 0 sets bit to output.



INTERRUPT CONTROL

Bit 7 = 1

interrupt enable is set—allowing interrupt to be generated.

Bit 7 = 0

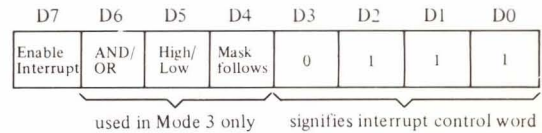
indicates the enable flag is reset and interrupts may not be generated.

Bits 6,5,4

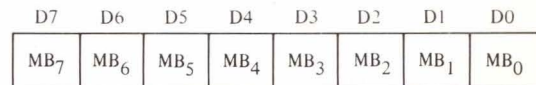
are used in the bit mode interrupt operations; otherwise they are disregarded.

Bits 3,2,1,0

signify that this command word is an interrupt control word.

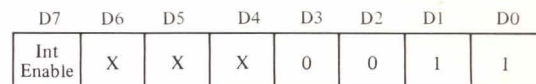


If the "mask follows" bit is high (D4 = 1), the next control word written to the port must be the mask.



Only those port lines whose mask bit is a 0 will be monitored for generating an interrupt.

The interrupt enable flip-flop of a port may be set or reset without modifying the rest of the interrupt control word by the following command.



$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5\text{ V} \pm 5\%$, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
Φ	t_C	Clock Period	400	[1]	nsec	
	$t_W(\Phi H)$	Clock Pulse Width, Clock High	170	2000	nsec	
	$t_W(\Phi L)$	Clock Pulse Width, Clock Low	170	2000	nsec	
	t_r, t_f	Clock Rise and Fall Times		30	nsec	
	t_h	Any Hold Time for Specified Set-Up Time	0		nsec	
CS, \overline{CE} ETC.	$t_{S\Phi}(\text{CS})$	Control Signal Set-Up Time to Rising Edge of Φ During Read or Write Cycle	280		nsec	
D_0-D_7	$t_{DR}(\text{D})$	Data Output Delay from Falling Edge of \overline{RD}	50	430	nsec	[2] $C_L = 50\text{ pf}$ [3]
	$t_{S\Phi}(\text{D})$	Data Set-Up Time to Rising Edge of Φ During Write or $\overline{M1}$ Cycle			nsec	
	$t_{DI}(\text{D})$	Data Output Delay from Falling Edge of \overline{IORQ} During INTA Cycle.		340	nsec	
	$t_F(\text{D})$	Delay to Floating Bus (Output Buffer Disable Time)		160	nsec	
IEI	$t_S(\text{IEI})$	IEI Set-Up Time to Falling Edge of \overline{IORQ} During INTA Cycle	140		nsec	
IEO	$t_{DH}(\text{IO})$	IEO Delay Time from Rising Edge of IEI		210	nsec	[5] [5] $C_L = 50\text{ pf}$ [5]
	$t_{DL}(\text{IO})$	IEO Delay Time from Falling Edge of IEI		190	nsec	
	$t_{DM}(\text{IO})$	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring Just Prior to $\overline{M1}$) See Note A.		300	nsec	
\overline{IORQ}	$t_{S\Phi}(\text{IR})$	\overline{IORQ} Set-Up Time to Rising Edge of Φ During Read or Write Cycle	250		nsec	
$\overline{M1}$	$t_{S\Phi}(\text{M1})$	$\overline{M1}$ Set-Up Time to Rising Edge of Φ During INTA or $\overline{M1}$ Cycle. See Note B.	210		nsec	
\overline{RD}	$t_{S\Phi}(\text{RD})$	\overline{RD} Set-Up Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	240		nsec	
A_0-A_7 , B_0-B_7	$t_S(\text{PD})$	Port Data Set-Up Time to Rising Edge of \overline{STROBE} (Mode 1)	260	230	nsec	[5] $C_L = 50\text{ pf}$ [5]
	$t_{DS}(\text{PD})$	Port Data Output Delay from Falling Edge of \overline{STROBE} (Mode 2)			nsec	
	$t_F(\text{PD})$	Delay to Floating Port Data Bus from Rising Edge of \overline{STROBE} (Mode 2)		200	nsec	
	$t_{DI}(\text{PD})$	Port Data Stable from Rising Edge of \overline{IORQ} During WR Cycle (Mode 0)		200	nsec	
\overline{ASTB} , \overline{BSTB}	$t_W(\text{ST})$	Pulse Width, \overline{STROBE}	150 [4]		nsec nsec	
\overline{INT}	$t_D(\text{IT})$	\overline{INT} Delay Time from Rising Edge of \overline{STROBE}		490	nsec	
	$t_D(\text{IT3})$	\overline{INT} Delay Time from Data Match During Mode 3 Operation		420	nsec	
ARDY, BRDY	$t_{DH}(\text{RY})$	Ready Response Time from Rising Edge of \overline{IORQ}		$t_C + 460$	nsec	[5] $C_L = 50\text{ pf}$ [5]
	$t_{DL}(\text{RY})$	Ready Response Time from Rising Edge of \overline{STROBE}		$t_C + 400$	nsec	

A. $2.5 t_C > (N-2) t_{DL}(\text{IO}) + t_{DM}(\text{IO}) + t_S(\text{IEI}) + \text{TTL Buffer Delay}$, if any

B. $\overline{M1}$ must be active for a minimum of 2 clock periods to reset the PIO.

[1] $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$

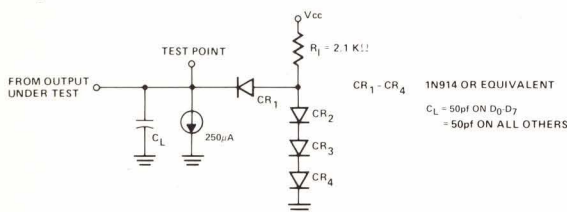
[2] Increase $t_{DR}(\text{D})$ by 10 nsec for each 50 pf increase in loading up to 200 pf max.

[3] Increase $t_{DI}(\text{D})$ by 10 nsec for each 50 pf increase in loading up to 200 pf max.

[4] For Mode 2: $t_W(\text{ST}) > t_S(\text{PD})$

[5] Increase these values by 2 nsec for each 10 pf increase in loading up to 100 pf max.

Output load circuit.



Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$

Symbol	Parameter	Max.	Unit	Test Condition
C_Φ	Clock Capacitance	10	pF	Unmeasured Pins Returned to Ground
C_{IN}	Input Capacitance	5	pF	
C_{OUT}	Output Capacitance	10	pF	

TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
Φ	t_c	Clock Period	250	[1]	nsec	
	$t_{WH}(\Phi H)$	Clock Pulse Width, Clock High	105	2000	nsec	
	$t_{WL}(\Phi L)$	Clock Pulse Width, Clock Low	105	2000	nsec	
	t_r, t_f	Clock Rise and Fall Times		30	nsec	
	t_h	Any Hold Time for Specified Set-Up Time	0		nsec	
CS, \overline{CE} ETC.	$t_{S\Phi}(CS)$	Control Signal Set-Up Time to Rising Edge of Φ During Read or Write Cycle	145		nsec	
D ₀ -D ₇	$t_{DR}(D)$	Data Output Delay From Falling Edge of \overline{RD}	50	380	nsec	[2]
	$t_{S\Phi}(D)$	Data Set-Up Time to Rising Edge of Φ During Write or $\overline{M1}$ Cycle			nsec	
	$t_{DI}(D)$	Data Output Delay from Falling Edge of \overline{IORQ} During INTA Cycle		250	nsec	[3]
	$t_F(D)$	Delay to Floating Bus (Output Buffer Disable Time)		110	nsec	
IEI	$t_S(IEI)$	IEI Set-Up Time to Falling edge of \overline{IORQ} During INTA Cycle	140		nsec	
IEO	$t_{DH}(IO)$	IEO Delay Time from Rising Edge of IEI		160	nsec	[5]
	$t_{DL}(IO)$	IEO Delay Time from Falling Edge of IEI		130	nsec	[5]
	$t_{DM}(IO)$	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring Just Prior to $\overline{M1}$) See Note A.		190	nsec	[5]
\overline{IORQ}	$t_{S\Phi}(IR)$	\overline{IORQ} Set-Up Time to Rising Edge of Φ During Read or Write Cycle.	115		nsec	
$\overline{M1}$	$t_{S\Phi}(M1)$	$\overline{M1}$ Set-Up Time to Rising Edge of Φ During INTA or $\overline{M1}$ Cycle See Note B	90		nsec	
\overline{RD}	$t_{S\Phi}(RD)$	\overline{RD} Set-Up Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	115		nsec	
A ₀ -A ₇ , B ₀ -B ₇	$t_S(PD)$	Port Data Set-Up Time to Rising Edge of \overline{STROBE} (Mode 1)	230		nsec	
	$t_{DS}(PD)$	Port Data Output Delay from Falling Edge of \overline{STROBE} (Mode 2)		210	nsec	[5]
	$t_F(PD)$	Delay to Floating Port Data Bus from Rising Edge of \overline{STROBE} (Mode 2)		180	nsec	
	$t_{DI}(PD)$	Port Data Stable from Rising Edge of \overline{IORQ} During WR Cycle (Mode 0)		180	nsec	[5]
\overline{ASTB} , \overline{BSTB}	$t_W(ST)$	Pulse Width, \overline{STROBE}	150 [4]		nsec nsec	
\overline{INT}	$t_D(IT)$	\overline{INT} Delay time from Rising Edge of \overline{STROBE}		440	nsec	
	$t_D(IT3)$	\overline{INT} Delay Time from Data Match During Mode 3 Operation		380	nsec	
ARDY, BRDY	$t_{DH}(RY)$	Ready Response Time from Rising Edge of \overline{IORQ}		$t_c + 410$	nsec	[5]
	$t_{DL}(RY)$	Ready Response Time from Rising Edge of \overline{STROBE}		$t_c + 360$	nsec	[5]

A. $2.5 t_c > (N-2) t_{DL}(IO) + t_{DM}(IO) + t_S(IEI) + \text{TTL Buffer Delay}$, if any

B. $\overline{M1}$ must be active for a minimum of 2 clock periods to reset the PIO.

[1] $t_c = t_{WH}(\Phi H) + t_{WL}(\Phi L) + t_r + t_f$

[2] Increase $t_{DR}(D)$ by 10 nsec for each 50 pf increase in loading up to 200 pf max.

[3] Increase $t_{DI}(D)$ by 10 nsec for each 50 pf increase in loading up to 200 pf max.

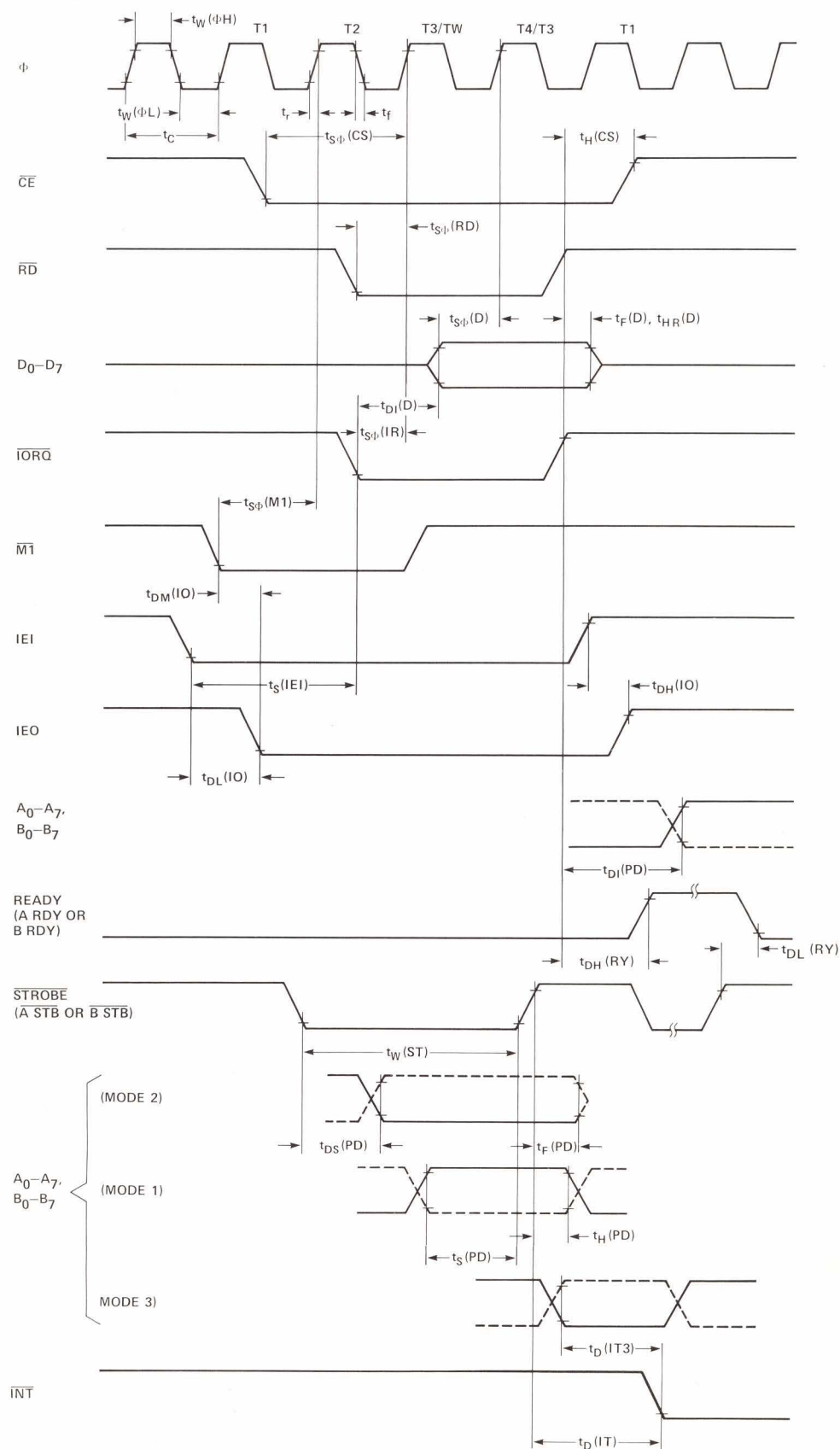
[4] For Mode 2: $t_W(ST) > t_S(PD)$

[5] Increase these values by 2 nsec for each 10 pf increase in loading up to 100 pf max.

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	= +0.5V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65° C to +150° C
Voltage On Any Pin With Respect To Ground	-0.3 V to +7 V
Power Dissipation	.6 W

***Comment**
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: All AC and DC characteristics remain the same for the military grade parts except I_{CC} .

$I_{CC} = 130\text{ mA}$.

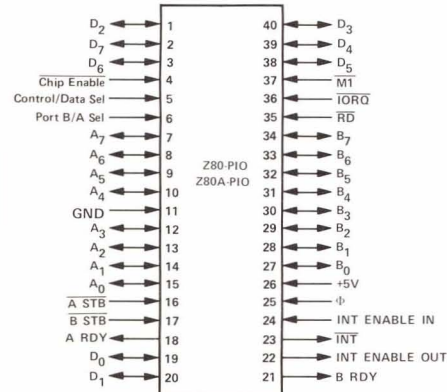
Z80-PIO and Z80A-PIO

D.C. Characteristics

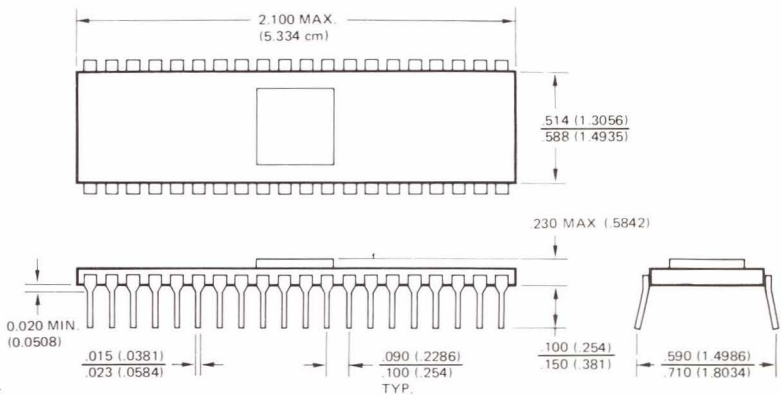
TA = 0° C to 70° C, Vcc = 5 V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V _{ILC}	Clock Input Low Voltage	-0.3	.45	V	I _{OL} = 2.0 mA I _{OH} = 250 μA
V _{IHC}	Clock Input High Voltage	V _{CC} -6	V _{CC} +3	V	
V _{IL}	Input Low Voltage	-0.3	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4	V	
V _{OH}	Output High Voltage	2.4		V	
I _{CC}	Power Supply Current		70	mA	V _{IN} = 0 to V _{CC} V _{OUT} = 2.4 to V _{CC} V _{OUT} = 0.4 V 0 ≤ V _{IN} ≤ V _{CC}
I _{LI}	Input Leakage Current		10	μA	
I _{LOH}	Tri-State Output Leakage Current in Float		10	μA	
I _{LOL}	Tri-State Output Leakage Current in Float		-10	μA	
I _{LD}	Data Bus Leakage Current in Input Mode		±10	μA	
I _{OH}	Darlington Drive Current	-1.5		mA	V _{OH} = 1.5 V Port B Only

Package Configuration



Package Outline



*Dimensions for metric system are in parentheses

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TWX 910 291 1064

WESTERN REGION

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TWX 910 595 1583

Intermark Electronics
4040 Sorrento Valley Blvd.
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714 453 9005
TWX 910 335 1515

Intermark Electronics
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TEL 408 738 1111
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TWX 910 498 2223

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Palo Alto, CA 94304
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C — Ceramic
P — Plastic
S — Standard 5V \pm 5% 0° to 70°C
E — Extended 5V \pm 5% -40° to 85°C
M — Military 5V \pm 10% -55° to 125°C

Example:

Z80-PIO CS (Ceramic—Standard range)

Zilog

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